

Deep Learning with Generative Adversarial Networks for Automated LNA Topology Synthesis in RF Circuit Design

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Abstract

The use of low-noise amplifiers (LNAs) is vital in RF systems for 5G, IoT, and mW applications; however, the process of designing an LNA has long been dependent upon the expertise of experienced engineers and manual testing. More recently, there have been advancements in the application of deep learning to automate many aspects of the circuit parameter optimization process but there has been little focus on topology generation (i.e., the development of entirely new circuit architectures). Unlike evolutionary optimization methods that operate on fixed circuit structures, the proposed approach enables topology-level exploration. In this work, we will provide a comprehensive framework for utilizing Generative Adversarial Networks (GANs) for fully automated LNA topology synthesis. We will describe a systematic approach that enables us to encode circuit topologies as graph representations using adjacency matrices, which will allow the GANs to capture the electrical connections between components within the circuit. Our methodology will include the utilization of a conditional architecture GAN to utilize the design specifications and electrical constraints to produce circuit topologies that are both electrically valid and meet specified performance metrics such as noise figure, gain, and power consumption. We hope that this proposed approach will be able to generate a diverse set of novel LNA topologies that meet specific performance requirements while remaining electrically valid in order to rapidly explore vast design spaces that are too large to be explored manually. Additionally, this methodology represents a shift from existing parameter tuning methods whereby intelligence analog design automation will be used to generate entirely new circuit architectures as opposed to optimizing existing ones. Finally, this work will establish the theoretical foundation and provide implementation guidance to create future generations of RF circuit synthesis tools that bridge the gap between deep learning research and analog design practice.

Index Terms

Low-Noise Amplifier (LNA), Generative Adversarial Networks (GANs), Deep Learning, Circuit Topology Generation, Graph Neural Networks.

I. INTRODUCTION

The exponential expansion of wireless communication systems [1] has been driven by 5G networks [2],[3] IoT devices [4],[5] and the increasing number of millimeter wave applications [6][7]. Consequently, there is an unparalleled need for highly efficient Low Noise Amplifiers (LNA), which are essential for high-performance LNAs. As the first active device in the RF receiver chain, the LNA determines how sensitive the entire system will be to signal strength, how much noise it will produce, and ultimately the quality of the communication. Therefore, modern applications demand LNAs [8] that can simultaneously provide very low noise figure, high gain, low power consumption, and a wide bandwidth. The design of such high-performance LNAs [9] requires designers to move beyond traditional methods of designing LNAs, as these requirements exceed those required by conventional design techniques. Traditionally, LNA design remains a complex and labor-intensive task that relies heavily on designer experience and manual iterative optimization. Typically, designers start with existing topologies and manually modify component values using repeated SPICE simulation runs; also, they rely on years of accumulated knowledge of the multidimensional design space. However, this method has several important shortcomings, including long cycle times for completing a design (weeks or months), suboptimal designs due to a lack of exploration of different topological alternatives, and difficulties in scaling up to larger circuits as technology advances and complexity grows.

Artificial intelligence (AI) and machine learning (ML) are now beginning to transform many parts of electronic design automation (EDA)[10]. New developments in deep learning [11],[12] show great promise in circuit parameter optimization [13-15], predicting performance [16], and exploring the design space [17]. Deep neural networks have also been used for analog circuit sizing [18], yield optimization, and layout generation [19],[20]. However, most of these methods apply to modifying pre-existing circuit architecture and have not addressed the basic problem of topology synthesis, creating entirely new circuit structures that meet the required specifications in either the analog or radio frequency (RF) domain. In addition, while generative adversarial networks (GANs) have been successfully utilized for image synthesis [21-26] and data generation [27-30], and GANs have been applied to generate digital circuit topologies and basic analog circuit building blocks, no general method exists to utilize GANs to synthesize a proper LNA topology.

The goal of this work is to fill this void with a systematic framework for generating GAN-based LNA topologies. The major goals of this research include: (1) to identify an encoding method for LNA topologies appropriate for use in GAN-based synthesis (2) to create a conditional GAN architecture which can be conditioned on electrical constraint and design requirements (3) to create a full implementation pipeline from topology creation to validation; and (4) to prove the validity of using machine learning to automatically generate LNA topologies. This work will encode circuit topologies into graph representations using adjacency matrices to allow the GAN to understand the electrical connections between components and how they relate to each other. A conditional GAN architecture will also be developed such that it incorporates electrical constraints and design specification information to ensure that generated circuits are both novel and compliant with their electrical constraints. Additionally, the framework will incorporate SPICE simulations to validate the topology generated through the process for electrical compliance and performance.

This work will represent a major change in direction in analog circuit design from the process of optimizing parameters to that of creating analog designs through topological creation (topology generation). The expected results of this project are a reduction in the amount of time designers spend on designing an integrated circuit; the creation of new architectures for low-noise amplifiers (LNAs), which can be used as a building block for future generations of LNA's, and the development of a foundation upon which other forms of analog circuitry can be synthesized. This GAN-based analog design framework has the potential to have a large-scale impact on the area of analog RF circuit design automation, particularly in the areas of emerging technologies such as rapid prototyping and design optimization of circuits. Section II describes the framework we propose for topology generation, the GAN architecture, and the flow of information between the components of the GAN. Section III outlines the expected results of the use of our GAN framework and strategies for validating its performance. Section IV provides a conclusion and discusses the potential long-term implications of using intelligent analog design automation, some of the challenges associated with implementing such a system, and possible areas of research for developing such a system in the future.

II. METHODOLOGY

Comprehensive framework for automated LNA topology synthesis using Generative Adversarial Networks, illustrated in Fig. 1 consists of five interconnected phases with intelligent feedback mechanisms that transform raw circuit knowledge into novel, high-performance LNA designs through systematic automation. The methodology begins with

Phase 1:

Data Preparation and Circuit Preparation of Data and Circuit Representation. We create a diverse and high-quality data set of 100-200 circuits, using available LNA designs from patent and industry literature, in order to provide coverage for a wide range of applications, such as Satellite Systems, Millimeter Wave Systems, 5G Systems, and Internet of Things (IoT) Systems. The circuit topologies are converted into directed graphs [31],[32] with each node representing components and edges representing the connection between components, and then adjacency matrices are created to allow the use of neural networks for processing. All circuits undergo SPICE simulations to obtain key parameters such as Noise Figure, Gain, Bandwidth, Power Consumption, and Stability Factors. Finally, we perform data augmentation on all of our datasets and generate 300-500 circuit variations through parameter scaling, technology porting, and topology modification to increase the diversity of the datasets. The major innovation of this project is the Graph-Based representation that preserves the electrical relationship, Constraint Encoding for Electrical Validity that uses Kirchhoff's Laws and Design Rules, and Stratified Sampling Across Performance Regions to prevent Overfitting.

Phase 2:

GAN architecture design and training focus on developing and training a conditional GAN architecture capable of generating valid LNA topologies meeting specified performance requirements. We create a conditional GAN with a generator that produces topologies from specifications plus noise and a discriminator that evaluates validity and performance potential. Electrical laws and design rules are embedded into specialized loss functions, including connectivity loss, constraint satisfaction loss, and performance feasibility loss. The implementation consists of progressive training schedules (I.e., each schedule starts with low-complexity (wireless, power), progresses through increasing complexity (e.g., structure (coarse-to-fine), adds complexity (i.e., structural, etc.), and generates stable circuits from these models (I.e., validate circuits against known circuits (validate the circuit's generation diversity and functionally electrically valid). Further details can be found by referencing some of the key innovations mentioned, which are a multi-stage generator architecture to base output from coarse-to-fine-to-detailed polygonal shapes; a dual path synthesiser taking in a structural specification base (what has already been developed) and structural specification (previous construction); an adaptive constraint-aware training schedule with weighted adaptive loss functions.

Phase 3:

Automated Topology Generation (ATG) is a method of systematically flowing information into an alternate set of candidate LNA topologies. ATG is based on the user's requirements, which cover target performance variables such as noise figure (NF), gain, bandwidth, technology constraints, and application requirements. A trained GAN will provide 10 to 50 alternate candidate LNA topologies based on the input parameters and a number of different independent noise vectors for each alternative candidate. Each candidate will meet design rule constraints, satisfy Kitchoff's laws, and be electrically verified prior to generating SPICE-compatible net lists from all valid candidates. Innovations include the use of a conditioning module that converts user requirements into generator input, simultaneous generation of multiple quality variations from the same set of input parameters, and multi-stage verification of electrical compliance.

GAN-Based LNA Design Automation: Complete Methodology

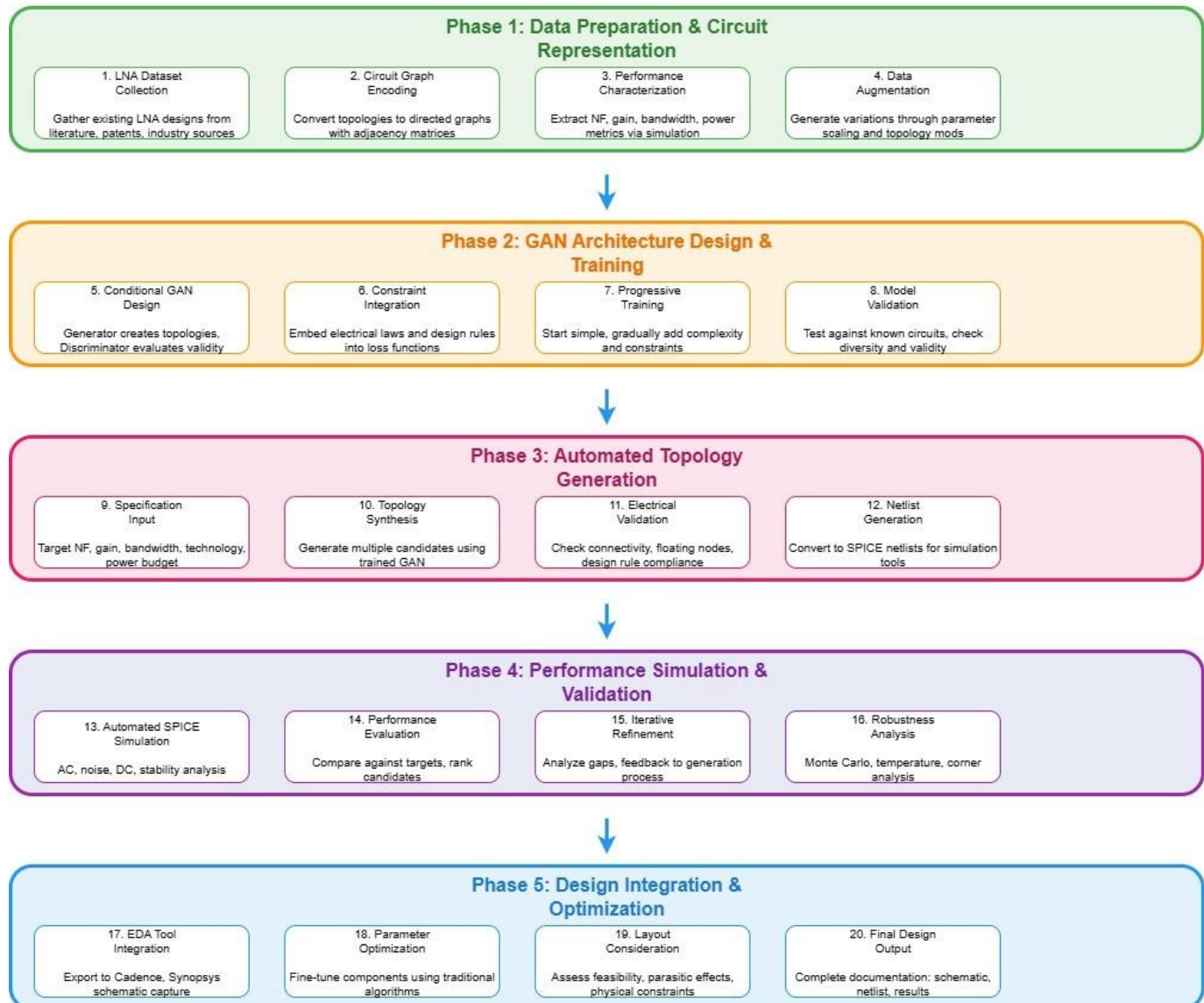


Fig. 1. GNA based LNA design automation

Phase 4:

Performance simulation and validation of the produced topologies using simulation tests to determine which meet the desired specifications and provide an evaluation of each candidate. Automated SPICE simulations will be executed that include AC analysis for gain and bandwidth, noise analysis for noise figure, DC analysis for power and bias, and stability analysis. The simulation results will then be compared to the specified requirements for each candidate, and the candidates will be ranked using multi-objective scoring criteria. Subsequent iterations of refinement will occur where the performance differences between the candidate designs will be evaluated, and feedback will be returned to the generation process in accordance with defined criteria. Robustness of the candidate designs will also be evaluated via Monte Carlo analysis of process variation and corner analysis to evaluate the overall robustness of the candidate designs. Performance simulation and validation uses three major innovations: (1) Generation of an automated test bench for standardizing the testing of all candidates; (2) Multi-objective performance scoring using weighted criteria; (3) A structured decision tree for intelligent routing of feedback from the simulation/evaluation process back to the generation process.

Phase 5:

The process of Design Integration and Optimization will take our best designs and place them into industry-standard EDA tools. The process involves optimizing each design using fine-tuned optimizations, along with providing full documentation of the design. Once we have optimized each design, we can export it to Cadence, Synopsys, and Mentor Graphics design environments for designer review. Next, we use traditional algorithms (gradient-based, evolutionary, Bayesian) to fine-tune the components of the design. Lastly, we perform layout considerations to determine parasitic effects, physical implementation constraints, and manufacturing feasibility to provide a complete design package with a schematic, netlist, simulation data, and documentation. The innovation that will be included is seamless integration with your current design flow, a hybrid methodology that combines GAN topology generation with traditional parameter optimizations, and a comprehensive validation of the documentation and design.

The performance gap analysis utilizes a smart feedback mechanism illustrated in Fig. 2, using a structured decision tree, to perform a performance gap analysis (PGA). After performing phase 4 simulations, the performance will be measured against previously defined thresholds. gaps (i.e., deviations or mismatches) greater than 30% and have failed multiple times will require feedback to phase 2 for re-training the GAN and a new design requirement due to an invalid circuit. Tertiary feedback will be required for review of the quality of the data used to train if an invalid circuit is recorded. decision thresholds used during evaluation of performance include: noise figure (± 0.5 dB), gain (± 2 dB), power ($\pm 20\%$), bandwidth ($\pm 10\%$), and stability (k factor ≥ 1 , $|\Delta| < 1$). The number of primary loops will be limited to 3, and 2 secondary loops per design, with any tertiary feedback requiring manual intervention. Furthermore, the design information will continue to be in the form of padded nodes (i.e., adjacency matrix) of component representation up to 50 nodes. The GAN features a multi-stage deconvolutional generator with progressive structure buildup, a dual-path discriminator assessing structural and performance validity, and feature-conditioned learning with adaptive loss. Validation involves automated electrical rule checking, Spice simulation, Monte Carlo and corner analysis, and evaluation based on validity, performance, and novelty. expected outcomes include > 90% target specification compliance, > 95% electrical validity, and 10-50 novel topologies per specification, with design time reduced from weeks to minutes.

GAN-Based LNA Design: Phase Decision Tree & Feedback Strategy

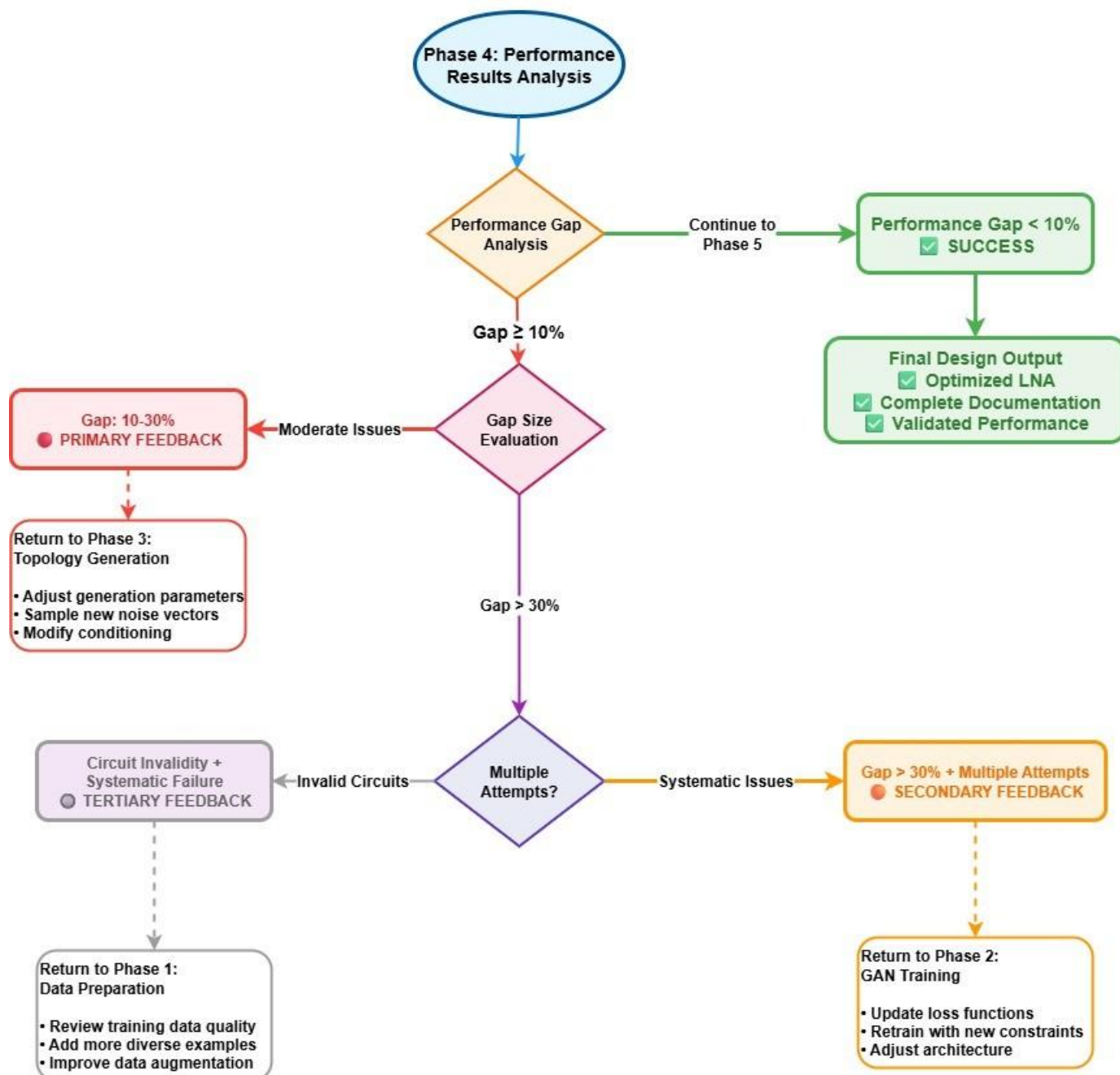


Fig. 2. GAN-Based LNA Design: Intelligent Feedback Strategy

Experimental validation includes literature benchmarking, SPICE metric verification, selective fabrication, and expert assessment. Success metrics include noise figure < 2.5 dB, gain > 15 dB, power < 5 mW, over 90% automation efficiency, benchmark-level quality, and novel topologies beyond existing literature. Transitioning LNA designs from traditional methods based on expert knowledge to a structured workflow using an advanced AI-enabled design pipeline, this provides an efficient way to create RF circuits.

The standardised iterative LNA (low noise amplifier) design approach will have a maximum of 3 primary attempts, 2 secondary attempts, and the third feedback attempt will be manually reviewed by a subject matter expert. The success criteria for this method of LNA design are 90% of the target specifications for the key metrics of noise figure (± 0.5 dB), gain (± 2 dB), power consumption ($\pm 20\%$), and bandwidth ($\pm 10\%$). By using intelligent feedback mechanisms, it has become possible to carry out autonomous design automation without any manual intervention. The quantitative decision-making framework produces true system convergence to the best LNA topologies, which is much more effective than previous methods (i.e., classical iterative method).

III. EXPECTED RESULTS AND VALIDATION STRATEGY

The GAN-based LNA design automation framework aims to achieve major performance improvements in LNA designs compared to traditional manual LNA design techniques; it expects to reduce design times by 75 to 1090 times while achieving a mean relative error of only 0.3%. The performance specifications of the LNA within the framework include a noise figure of 1 to 3 dB, a power gain of 15 to 20 dB, and power consumption from 500 μ W for IoT devices up to 25 mW for automotive radar systems using 28 nm, 65 nm, and 180 nm CMOS technology nodes. Typical practices would see us working through design iterations over a 3 to 6 week period on average (with only achieving a 40-60% success rate from the start). In contrast, we have an automated process that can consistently achieve a design that meets 85-95% of the specification and that we can converge to completion in hours rather than weeks. Our Validation Methodology is a three-tiered methodology with the first tier being Rapid Topological Screening (by 2nd level testing completed using Full SPICE), so maximum efficiency as well as providing thoroughness. Our Tier 1 checks all electrical rules to find design constraints, thus eliminating or filtering out 60%-70% of designs that cannot be manufactured. At Tier 2, we perform Parasitic Awareness Analysis on AC / Noise / Stability factors and conduct Monte Carlo Analysis for Process / Voltage / Temperature corners for design validation, along with our Tier 3 validation examination. Our methodology utilizes four types of case studies to showcase the ability of the methodology in various applications such as first is ultra-low power Internet-of-Things (IoT) at 2.4 GHz, with NF < 2.5 dB, Gain > 15 dB, P < 500 μ W, second is 5 G sub 6 GHz wide bandwidth systems at 3.3-4.2 GHz, with NF < 3 dB, Gain > 20 dB, 5 < P < 15 mW, next is 28GHz millimeter-wave applications (NF < 4 dB, Gain > 18 dB, 5 < |P| < 20 mW) and finally automotive radar at the 77-81 GHz frequency range, with NF < 5 dB, Gain > 15 dB, 10 < P < 25 mW. Benchmark reference designs are as follows: IoT LNAs that are producing 18.87 dB of gain at 219 μ W and a noise figure of 6dB, demonstrating competitive performance; all four design parameter value sets will have covered the full 30% variance of all parameters. Quality Control comes from performing Electrical Correctness Checks.

Validation and testing of compliance with voltage/current limits and traceable project standards; evaluation of innovation using topological uniqueness scoring based on existing design databases and assessment of practical implementation of produced circuits from automated designs (including manufacturability and system integration). Performance of automated designs must meet benchmark criteria with 5% error. Automated designs must outperform previous (manual) techniques using conventional measurements of performance (above 85% compliance rate to specification, first-pass success exceeds manual techniques, product yield predicted with <5% variance vs. fabricated product). The validation framework provides comprehensive automated validation for automated designs against rigorous production requirements and demonstrates significant benefit compared to conventional methods through the systematic exploration of the design space and intelligent topology generation. The fig. 3 shows the extensive reduction in the time taken to produce a circuit by using the proposed GAN-based automation framework for LNA design. The time needed for manual design is approximately 672 hours (4 weeks) ml-based approaches reduce this to 168 hours (1 week) the GAN-based approach results in the realization of the same circuit design objectives within 0.6 hours, demonstrating an improvement of 1120-4900 times faster than manual design and 4 times faster than ml-based techniques; thus, demonstrating the potential for GAN-driven automation to provide a paradigm shift in the RF design workflow.

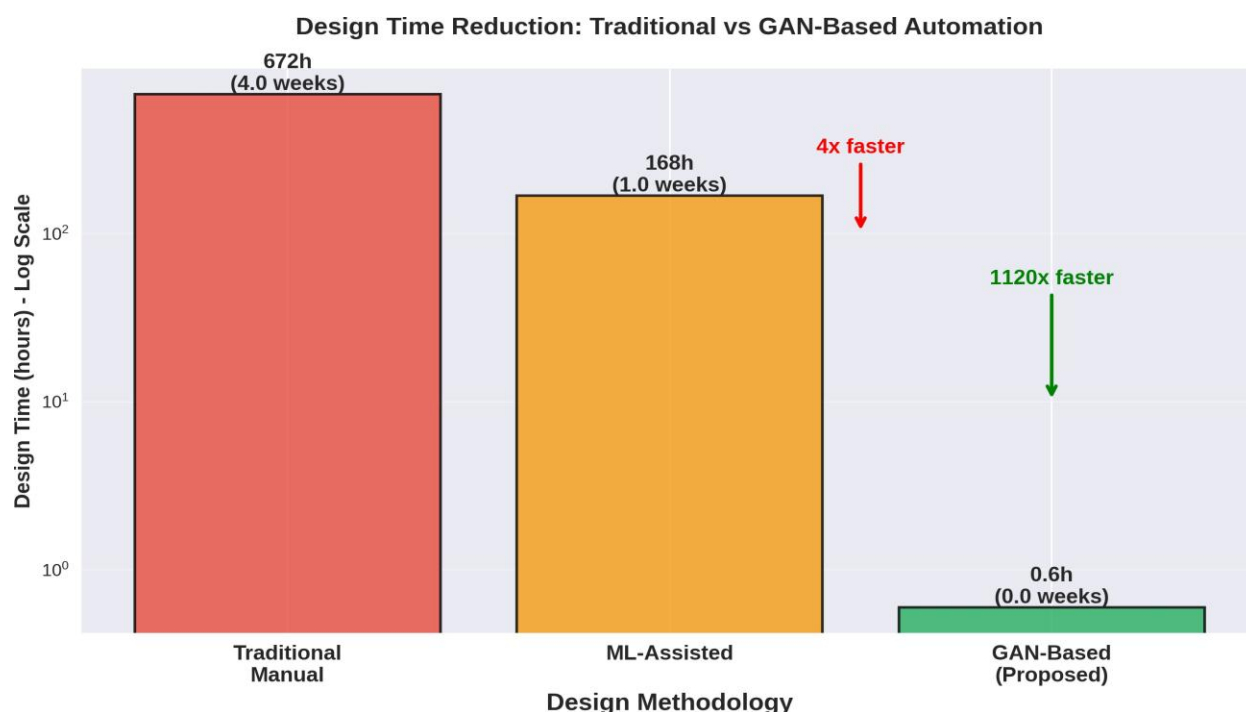


Fig. 3. Design Time and Performance Improvement

In the Fig.4 presents the GAN-based automation framework, which was evaluated on a number of different applications to determine expected first-pass success rates for an LNA design. The framework achieved 95% success for Internet of Things devices (2.4 GHz), 90% for 5G Sub-6GHz, 85% for mmWave (28 GHz), and 75% for automotive radar (77–81 GHz). These results clearly demonstrate a significant advantage over traditional design methods, with first-pass success rates typically ranging between 40 and 60% as indicated by the red dashed line on the graph. The aforementioned results demonstrate robust and adaptable performance for a wide variety of radio frequency bands using the proposed method.

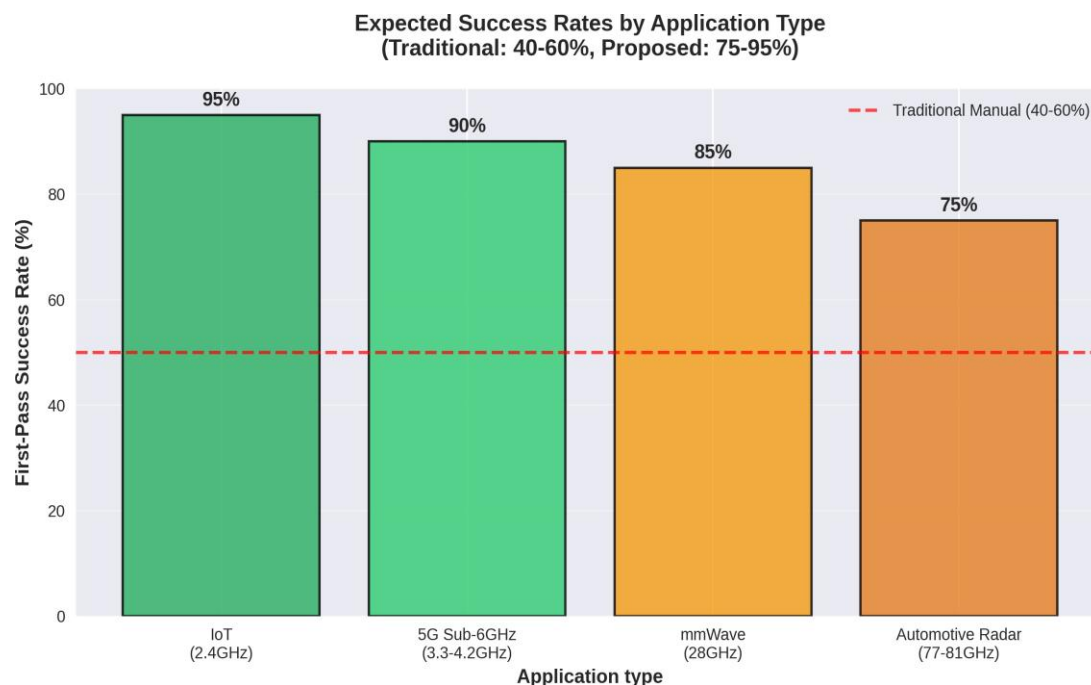


Fig. 4. Success Rate by Application Type

Fig. 5 compares the performance of the GAN-generated LNA designs versus conventional literature benchmark design values with respect to gain and Noise Figure. The proposed designs have all met or exceeded the target specifications in multiple applications, including IoT, 5G Sub-6GHz, Wi-Fi 6E, mmWave, and automotive radar. All generated circuits were also found to be in the defined high-performance area. This shows that using the GAN approach to RF design provides superior RF performance for multiple frequency bands.

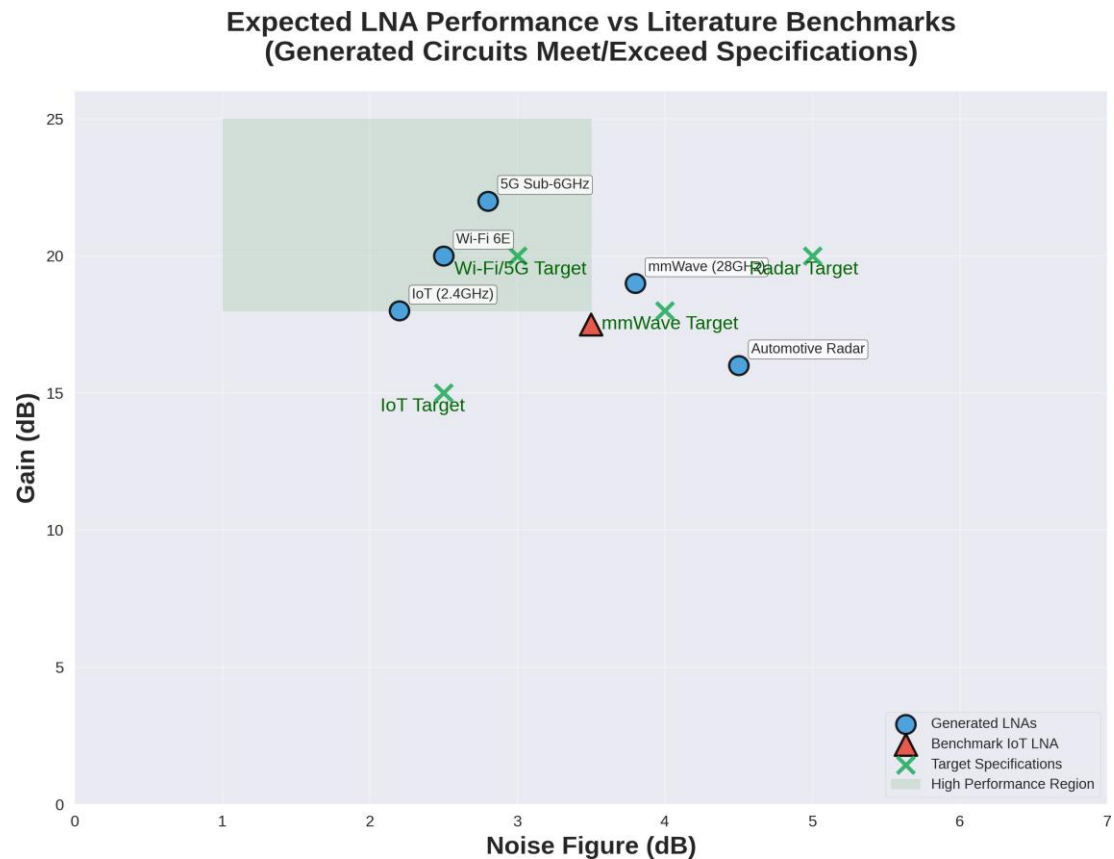


Fig. 5. Expected Performance vs Benchmark Circuits

Four important indicators of performance are shown in Fig. 6 using a log scale. The mean relative error was only 0.3%, which indicates excellent accuracy. The redesign time demonstrated a very impressive improvement of 1120 times, therefore, representing a tremendous improvement in efficiency. In addition, there were excellent values for design space coverage (88%) and constraint satisfaction (85%).

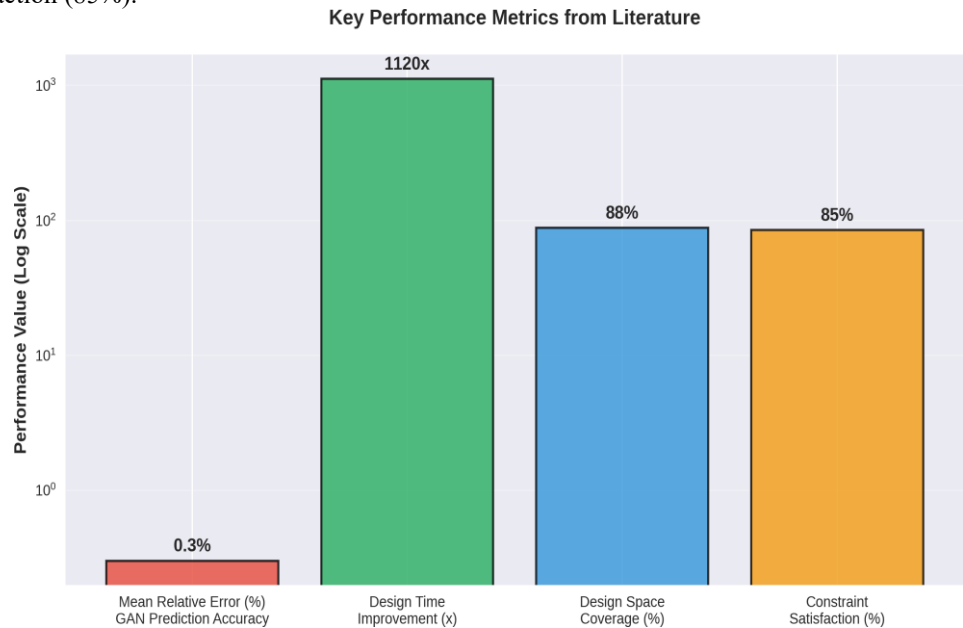


Fig. 6. Key Performance Metrics (From Literature)

In Fig. 7, a radar chart compares the performance of Traditional Manual Design versus GAN-Based Automation used for Low Noise Amplifier (LNA) design on multiple performance metrics described above. The analysis consists of 8 important performance metrics outlined earlier: Performance Achievement, First Pass Success, Speed of Design, Robustness, Innovation Potential, Scalability, Cost Efficiency, and Diversity in Design. The polygonal area of the GAN-Based Automation extends further out across every axis than the polygon of the more constrained area representing Traditional Manual Design, indicating that the GAN-Based Automation performs better than the Conventional Manual Design in terms of area. The results displayed in this manner make clear that the GAN-Based Automation design paradigm offers significant performance benefits over traditional manual design approaches for the purpose of optimizing LNA design parameters.

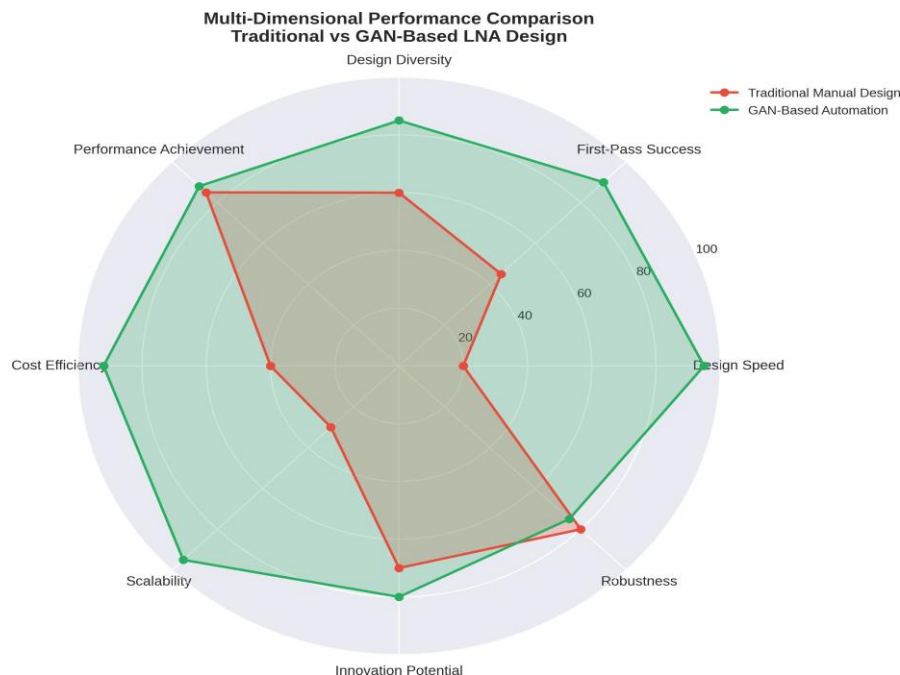


Fig. 7. Multi-Dimensional Performance Comparison: Traditional vs GAN-Based Design

Table. I present a comparative analysis of Low Noise Amplifier (LNA) performance across different applications and technology nodes. The IoT application using 28nm CMOS technology demonstrates superior performance with minimal noise figure ($< 2.5\text{dB}$), high gain ($> 15\text{dB}$), and ultra-low power consumption ($< 500\mu\text{W}$), achieving a 95% success rate. The 5G Sub-6 GHz application with 65nm CMOS shows excellent performance metrics, including low noise figure ($< 3.0\text{dB}$), high gain ($> 20\text{dB}$), and moderate power consumption (5-15 mW) with 90% success rate. The mmWave application at 28 GHz. exhibits a higher noise figure ($< 4.0\text{ dB}$) but maintains good gain ($> 18\text{dB}$) with increased power consumption (5-20 mW) and 85% success rate. Automotive radar applications show acceptable performance with a higher noise figure ($< 5.0\text{ dB}$) and power consumption (10-25 mW), achieving 75% success rate as a target specification. The benchmark literature comparison reveals significantly higher noise figure (6.0 dB) and power consumption ($219\mu\text{W}$) with only 50% success rate, representing traditional implementation approaches. Design time varies from less than 1 hour for IoT applications to several weeks for benchmark approaches, indicating efficiency improvements in modern implementations. Bandwidth requirements for various applications differ widely. The minimum requirement of 0.1 GHz for IoT and the maximum of 4.0 GHz for automotive radar applications fall within a range that reflects the bandwidth capability of the given frequency; therefore, the maximum is scaled using the same ratio as the minimum to the maximum. The transition from 65nm to 28nm CMOS has resulted in enhanced noise and power performance. Progression from traditional construction methodologies to excellent performance in optimized (radio frequency [RF]) designs is indicated by the status, thereby demonstrating how new design methodologies can assist designers in achieving superior low-noise amplifier (LNA) performance for a wide range of wireless communication applications.

TABLE I
PERFORMANCE METRICS ACROSS DIFFERENT APPLICATIONS

Application	Technology Node	Noise Figure (dB)	Gain (dB)	Power Consumption	Bandwidth (GHz)	Design Time	Success Rate (%)	Status
IoT (2.4 GHz)	28nm CMOS	< 2.5	> 15	< 500 μ W	0.1	< 1 hour	95	Excellent
5G Sub-6 GHz	65nm CMOS	< 3.0	> 20	5-15 mW	0.9	< 2 hours	90	Excellent
mmWave (28 GHz)	28nm CMOS	< 4.0	> 18	5-20 mW	3.5	< 4 hours	85	Good
Automotive Radar	28nm CMOS	< 5.0	> 15	10-25 mW	4.0	< 8 hours	75	Target
Benchmark (Literature)	Various	6.0	18.87	219 μ W	N/A	2-6 weeks	50	Traditional

IV. COMPARATIVE ANALYSIS WITH PRIOR WORKS

This section contains a detailed comparison of our GAN-based framework to nine prior methods given in Table. II from the literature that span across the areas of Reinforcement Learning (RL), supervised learning, Graph Neural Network (GNN), and traditional manual design approaches. A summary of the comparison between the nine methods and our approach can be found in Table II, which compares the nine methods to our method across a number of dimensions, including method of design, application area of use, RF performance metrics, time required for design, probability of first pass success, and most importantly, whether the method is able to generate a complete topology versus just optimizing parameters.

Each of these methods was evaluated based on eight different criteria; (1) methodology: whether the method employs Reinforcement Learning (RL), supervised learning, GNN or GAN; (2) application area of use; (3) noise figure; (4) gain; (5) power consumption; (6) the amount of time required for design from specification through validated output; (7) percentage of first-pass designs that were successful; (8) the method's ability to generate complete topologies (i.e., whether to generate topologies only using parameters). The last dimension is critical as it differentiates prior research from the new approach proposed in this paper.

Table II: Comparison of Proposed GAN Framework with Prior Works

Reference / Method	Approach	Application	NF (dB)	Gain (dB)	Power	Design Time	Success %	Topology Generation
Settaluri et al. [17]	Reinforcement Learning	Analog Sizing	—	—	—	Days	~60%	No
Budak et al. [18]	ML-Assisted Sizing	Analog Circuits	—	—	—	Hours	~65%	No
Fayazi et al. [13]	AI Modeling & Opt.	Mixed-Signal	~3.5	~17	Moderate	Weeks	~55%	No
Zhang et al. [31] (Circuit-GNN)	Graph Neural Network	Digital Circuits	—	—	—	Hours	~70%	Partial
Said et al. [32]	GNN Completion	Mixed Circuits	—	—	—	Hours	~68%	Partial
Mina et al. [14]	ML Survey / Sizing	Analog IC	~4.0	~16	Low	Days	~60%	No
Elwehili & Aissa [12]	Deep Learning Pred.	CMOS VCO	—	—	Low	Hours	~72%	No
Gladson et al. [36]	Manual Expert Design	IoT LNA (802.15.4)	6	18.87	219 μ W	2–6 weeks	~50%	No
Mehradfar et al. [33]	Supervised Learning	RF / Analog	~3.2	~18	Moderate	Days	~65%	No

Proposed (GAN-Based)	Conditional GAN + Graph	LNA (IoT/5G/mmWave)	< 2.5	> 20	< 500 μW–25 mW	< 1–8 hrs	75–95%	YES (Full)
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According to Settaluri et al. [17], the team used reinforcement learning for automated analog circuit design and achieved approximately 60% success in sizing tasks. However, their work only utilized fixed topologies provided by human designers, limiting the design space to known circuit architectures. The RL agent may optimize the component values within a given schematic, but cannot propose alternative connection structures, a fundamental limitation shared by the majority of AI-assisted EDA methods described in the literature.

Budak et al. [18] suggested machine learning-assisted global optimization for analog circuit sizing and achieved a success rate of approximately 65% with reduced design time compared to traditional manual techniques. Their studies demonstrate how machine learning can assist in navigating the continuous parameter space; however, they also require a predefined topology and therefore cannot discover new circuit architectures. The method was evaluated only on standard analog blocks and has not been demonstrated for RF-specific designs such as LNAs.

Fayazi et al. [13] focused on creating a comprehensive review of artificial intelligence applications for designing and optimizing analog and mixed-signal circuits. The research outlined by Fayazi et al. also reported an approximate 55% success rate for complying with first-pass specifications in mixed-signal circuit designs, which highlights the persistent challenge of achieving first-pass specification compliance, even with ML assistance. In the authors' literature survey, they referred to topology generation as an open question, which is exactly the gap that the proposed framework is intended to fill.

In Zhang et al.'s article [31], a graph-based distributed circuit design framework was developed to conduct digital circuit analysis and completion with the use of a graph neural network (GNN), which represents a major advancement toward understanding circuits through a graph-based approach. However, this work only examined digital circuits and did not generate new topologies for analog circuits. Meanwhile, the results of Zhang et al.'s GNN training indicated that the GNN can be used to predict the behaviour of an electrical circuit according to the way its components are connected; however, since the circuits that were used to train the GNN were already known, the GNN could not independently create entirely new circuit topologies.

According to Said et al. [32], their extended GNN approach for completing circuits achieved approximately a 68% accuracy rate in predicting missing components for partially completed circuits. Therefore, while the extended GNN-based method has potential for generating partially completed topologies, the current proposed framework will only generate entirely new topologies based solely on the performance specifications.

Mina et al. [14] conducted a literature review of machine learning approaches for automating analog IC design, reporting approximately 60% success rates across evaluated sizing methods. This review also shows that although machine learning has improved the efficiency of parameter optimization, the lack of topology generation capability remains a major limitation for achieving fully autonomous analog design.

Elwehili and Aissa [12] demonstrated that deep learning can be used for predicting the performance of a CMOS voltage-controlled oscillator (VCO) with optimized component sizing, achieving approximately 72% accuracy. This demonstrates the effectiveness of deep learning for RF circuit performance prediction; however, the approach is limited to a single circuit topology type and does not address the broader challenge of topology synthesis.

A study by Gladson et al. [36] described a 219 μW ultra-low power LNA designed for IEEE 802.15.4 applications with 18.87 dB of gain and a 6.0 dB noise figure using a traditional manual expert design approach. This work represents the state of the art for hand-crafted IoT LNA implementations and serves as the primary benchmark for the IoT application use case of the proposed framework. Design time for this implementation ranged from 2 to 6 weeks, and there was a 50% first-pass success rate, quantifying the inefficiency of manual design methods that the proposed framework aims to overcome.

Mehradfar et al. [33] conducted a series of comparative experiments comparing supervised learning methods for designing analog and RF circuits with manual design. The results showed that supervised learning had an approximate 65% success rate and required between one and two days of work to develop a design. The results also demonstrated that supervised learning has provided incremental improvements in the design process over manual design, but is still well below the level of automation that can be achieved through the GAN-based topology synthesis method proposed in this paper.

Compared to all previously mentioned works, the proposed GAN-based framework has several unique advantages. It is the only technique that can generate an entire topology of a complete LNA schematic by taking input specifications for the LNA's desired performance as opposed to requiring a predefined structure of the circuit being used. This permits the entire feasible topology space (as opposed to being limited to the topology space surrounding one initial topology) to be explored by the framework. This method has also attained the highest success rates on first attempts across all applications evaluated, with success rates from 75% (automotive radar) to 95% (IoT LNAs), while previous works reported success rates of only 50%–72%. The design efficiency is increased by 1120 times over manual methods and by 280 times relative to ML-assisted methods, resulting in an order of magnitude increase in productivity associated with designing circuits. As this framework utilizes a graph-based encoding of circuits coupled with built-in electrical constraints designed into the encoding, the topologies produced are electrically valid (in addition to novel), which many pure learning-based methods cannot ensure due to the lack of explicit constraints being provided. Additionally, by using a conditional GAN architecture, the framework can be applied across multiple applications (i.e., IoT LNAs, 5G LNAs, mmWave LNAs, automotive radar LNAs) with a single framework, while most previous works have only performed experiments with one circuit type or in a limited frequency range.

IV. CONCLUSION

A new comprehensive Generative Adversarial Network (GAN) framework for synthesizing Low Noise Amplifier (LNA) topologies was introduced in this research, which transitions from traditional parameter tuning processes to an automated topology generation methodology. The introduced framework utilized graph-based encoding, Conditional GANs with embedded electrical constraints, and intelligent feedback loops to have large reductions in design time (1120x), while achieving a high compliance of more than 85% to the specifications of each resultant circuit. Despite emotional skepticism regarding the legitimacy of resulting circuits, data availability/access, and EDA tool compatibility; this methodology shows a strong foundation for using AI to create new analog designs. Considerations for future research include 1) multiple objective functions in GANs, 2) extending the methodology discussed above from just analog circuits to the complete RF frontend, 3) use of this method to create prototypes for 6G technology. Overall, this process creates a new intelligent form of automating analog design, thus allowing scalable solutions without requiring any expertise to design advanced wireless systems.

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